REMARKS

Summary of Office Action

Claims 1-37 were pending in the above-identified patent application.

Claims 1–3, 6-10, 16-19 and 22-26 were rejected under 35 U.S.C. § 103(a) as being obvious from Lee et al. U.S. Patent No. 6,266,799 (hereinafter "Lee") in view of Tanji et al. U.S. Patent No. 6,307,906 (hereinafter "Tanji").

Claim 11 was rejected under 35 U.S.C. § 103(a) as being obvious from Lee in view of Tanji in further view of Li et al. U.S. Patent No. 6,693,985 (hereinafter "Li").

Claims 12-15 were rejected under 35 U.S.C. § 103(a) as being obvious from Lee in view of Tanji and Li in further view of Wang et al. U.S. Patent No. 6,292,116 (hereinafter "Wang").

Claims 4, 5, 20, 21 and 27-37 were objected to as being dependent upon a rejected base claim.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of Applicants' Reply

Applicants note with appreciation the indication of allowability of the subject matter of claims 4, 5, 20, 21, and 27-37. Applicants expressly reserve the right to rewrite these claims in independent form should their base claims ultimately not be allowed.

Claims 1-37 were pending in the present application. In this Reply, applicants make no claim

amendments. Accordingly, claims 1-37 continue to be pending in the present application.

Applicants submit that claims 1-37 are allowable, as discussed below.

Reply to the Rejections
Under 35 U.S.C. 103(a)

Claims 1–3, 6-10, 16-19 and 22-26 were rejected under 35 U.S.C. § 103(a) as being obvious from Lee in view of Tanji. Claim 11 was rejected under 35 U.S.C. § 103(a) as being obvious from Lee in view of Tanji in further view of Li. Claims 12-15 were rejected under 35 U.S.C. § 103(a) as being obvious from Lee in view of Tanji and Li in further view of Wang. These rejections are respectfully traversed.

Claims 1-24

Applicants' invention, as defined by independent claims 1 and 16, is directed to circuitry and a method for extracting data from a data signal having a data rate that is twice the frequency of a reference clock signal. A first phase-shifted version of the reference clock signal is derived that is synchronized with a rising edge (i.e., a 0-to-1 level transition) of the data signal. The data signal is sampled in a predetermined phase relationship to this first phase-shifted version to extract a first partial stream of data. A second phase-shifted version of the reference clock signal is also derived that is synchronized with a falling edge (i.e., a 1-to-0 level transition) of the data signal. The data signal is further sampled in a

predetermined phase relationship to this second phase-shifted version to extract a second partial stream of data.

As admitted on page 3 the Office Action, Lee does not show or suggest "first circuitry to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal that are respectively synchronized with oppositely polarized transitions in level of the data signal" as recited in applicants' independent claims 1 and 16. The Office Action relies on Tanji to make up for the deficiencies in Lee.

Tanji refers to a clock and data recovery scheme for multi-channel data communication receivers. Tanji describes a system operative to measure the phase differences between a single reference clock signal and multiple data signals received by a multi-channel receiver. The system of Tanji outputs "a single clock signal to re-time all of the multiple channel data and is thereby able to reduce the jitter and channel crosstalk that can occur with multiple clocks" (col. 1, lines 40-44).

The Office Action alleges that Tanji describes "first circuitry (FIG. 1 elements 14 and 18, FIGS. 4A and 4B) configured to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal (FIG. 4A and 4B) that are respectively synchronized with oppositely polarized transitions in level of the data signal" (Office Action, pages 3-4). However, neither of elements 14 and 18

produce clock signals, much less first and second phase-shifted versions of the reference clock signal that are respectively synchronized with oppositely polarized transitions in level of the data signal. Data sampler 14 merely produces a synchronized copy DATA OUT of a data signal, while phase detector 18 produces aperiodic output control signals UPN and DOWN. None of the DATA OUT, UPN and DOWN signals are clock signals respectively synchronized with oppositely polarized transitions in the data signal.

In addition, applicants submit that Tanji teaches away from deriving multiple clock signals respectively synchronized with oppositely polarized transitions in the data signal. The system of Tanji teaches the use of a single clock signal to replace multiple clock signals in order "to reduce the jitter and channel crosstalk that can occur with multiple clocks" (col. 1, lines 40-44), and to reduce the power consumption and chip area required by multiple clocks (col. 5, lines 28-35). If anything, Tanji teaches the use of a single clock signal synchronized with a data signal instead of the claimed multiplicity of clock signals synchronized with oppositely polarized transitions in the data signal.

For at least the foregoing reasons, applicants respectfully submit that independent claims 1 and 16 are allowable. Claims 2-15 and 17-24, which depend from independent claims 1 and 16, respectively, are therefore also allowable.

Claims 25-37

Applicants' invention, as defined by independent claim 25, is directed to an apparatus for receiving an information signal that includes data information and clock information for the data information embedded in the information signal. The apparatus includes first input circuitry to receive the information signal and second input circuitry to receive a reference clock signal. Reference clock signal processing circuitry produces two recovered clock signals based on the information signal and the reference clock signal, the recovered clock signals respectively synchronized with oppositely polarized transitions in level of the information signal. Data recovery circuitry produces two retimed data output signals indicative of the data information in the information signal based on the information signal and the two recovered clock signals.

For at least the reasons given above with respect to independent claims 1 and 16, applicants respectfully submit that independent claim 25 is also allowable. Claims 26-37, which depend from independent claim 25, are therefore also allowable.

Conclusion

Applicants respectfully submit that this application, including claims 1-37, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully Submitted,

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